CLAIMS

What is claimed is:

1. A die, comprising:

a first conductor carrying a power supply voltage;

a second conductor carrying a ground voltage; and

at least one semiconductor capacitor operating in depletion mode coupled between the first and second conductors to provide decoupling capacitance between the first and second conductors, the at least one semiconductor capacitor having a gate voltage.

2. The die of claim 1, wherein the at least one semiconductor capacitor has a n+ gate poly and n+ source/drain regions in an n-body.

3. The die of claim 1, wherein the at least one semiconductor capacitor has a p+ gate poly and n+ source/drain regions in an n-body.

4. The die of claim 1, wherein the at least one semiconductor capacitor has a p+ gate poly and p+ source/drain regions in an n-body.

5. The die of claim 1, wherein the at least one semiconductor capacitor has a p+ gate poly and p+ source/drain regions in a p-body.

6. The die of claim 1, wherein the at least one semiconductor capacitor has a n+ gate poly and p+ source/drain regions in a p-body.

7. The die of claim 1, wherein the at least one semiconductor capacitor has a n+ gate poly and n+ source/drain regions in a p-body.

8. The die of claim 1, wherein the power supply voltage has a smaller absolute value than does a flatband voltage.

9. The die of claim 1, further comprising voltage circuitry to provide a body voltage to the at least one semiconductor capacitor and wherein the gate voltage is provided by the first conductor.

10. The die of claim 1, further comprising voltage circuitry to provide a body voltage to the at least one semiconductor capacitor and wherein the gate voltage is provided by the second conductor.

11. The die of claim 1, further comprising voltage circuitry to provide the gate voltage and wherein a body voltage of the at least one semiconductor capacitor is provided by the first conductor.

12. The die of claim 1, further comprising voltage circuitry to provide the gate voltage and wherein a body voltage of the at least one semiconductor capacitor is provided by the second conductor.

13. The die of claim 1, further comprising additional capacitors between the first and second conductors at least some of which are not in the depletion mode.

14. A die, comprising:

a first conductor carrying a power supply voltage (Vcc);

a second conductor carrying a ground voltage (Vss); and

capacitors having:

(a) a conductive gate;

(b) an insulator dielectric;

(c) a semiconductor body,

wherein, the capacitor is in a depletion mode.

15. The die of claim 14, wherein the capacitors have a n+ gate poly and n+ source/drain regions in an n-body.

16. The die of claim 14, wherein the capacitors has a p+ gate poly and n+ source/drain regions in an n-body.

17. The die of claim 14, wherein the capacitors has a p+ gate poly and p+ source/drain regions in an n-body.

18. The die of claim 14, wherein the capacitors has a p+ gate poly and p+ source/drain regions in a p-body.

19. The die of claim 14, wherein the capacitors has a n+ gate poly and p+ source/drain regions in a p-body.

20. The die of claim 14, wherein the capacitors has a n+ gate poly and n+ source/drain regions in a p-body.

21. The die of claim 14, wherein the power supply voltage has a smaller absolute value than does a flatband voltage.

22. A die, comprising:

a first conductor carrying a power supply voltage;

a second conductor carrying a ground voltage; and

at least one semiconductor capacitor coupled between the first and second conductors to provide decoupling capacitance between the first and second conductors, the semiconductor capacitor having a gate voltage, the semiconductor capacitor having a flatband voltage and wherein the power supply voltage has a smaller absolute value than does the flatband voltage.

23. The die of claim 22, wherein the at least one semiconductor capacitor has a n+ gate poly and n+ source/drain regions in an n-body.

24. The die of claim 22, wherein the at least one semiconductor capacitor has a p+ gate poly and n+ source/drain regions in an n-body.

25. The die of claim 22, wherein the at least one semiconductor capacitor has a p+ gate poly and p+ source/drain regions in an n-body.

26. The die of claim 22, wherein the at least one semiconductor capacitor has a p+ gate poly and p+ source/drain regions in a p-body.

27. The die of claim 22, wherein the at least one semiconductor capacitor has a n+ gate poly and p+ source/drain regions in a p-body.

28. The die of claim 22, wherein the at least one semiconductor capacitor has a n+ gate poly and n+ source/drain regions in a p-body.

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